



KD2319SRG

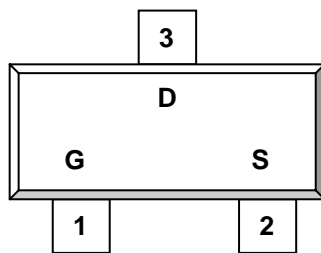
P Channel Enhancement Mode MOSFET

DESCRIPTION

-3.0A

KD2319SRG is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are required in a very small outline surface mount package.

PIN CONFIGURATION SOT-23

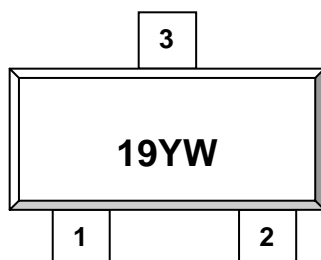


1.Gate 2.Source 3.Drain

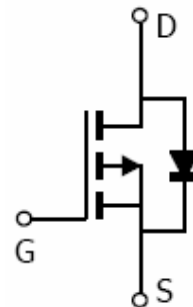
FEATURE

- -40V/-3.0A, $R_{DS(ON)} = 75m\Omega$ (Typ.) @VGS = -10V
- -40V/-2.8A, $R_{DS(ON)} = 105m\Omega$ @VGS = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PART MARKING SOT-23



Y: Year Code W: Week Code



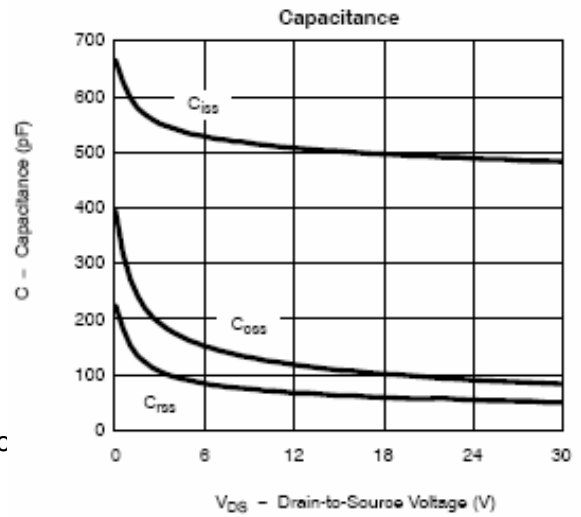
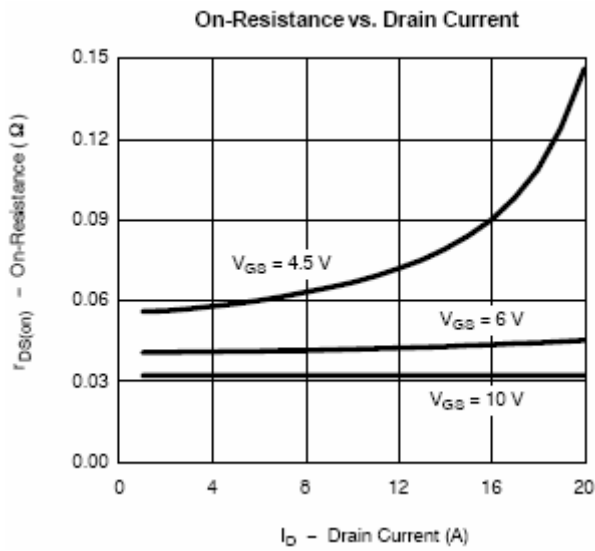
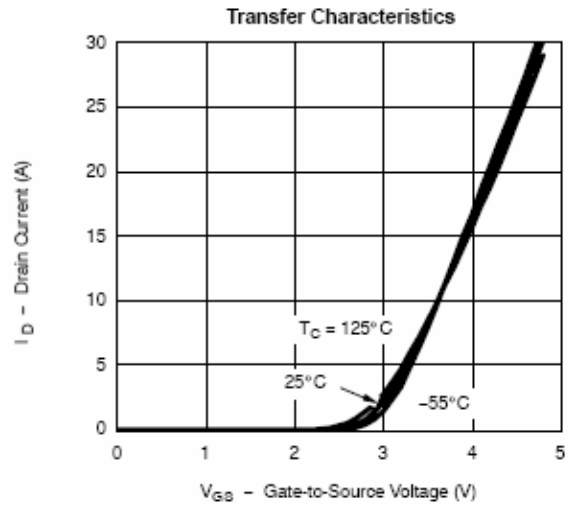
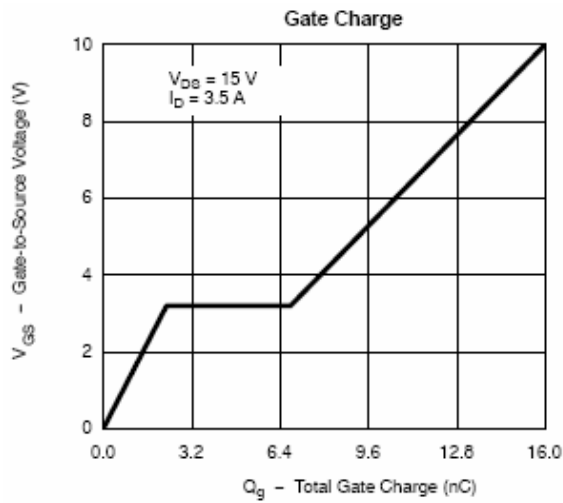
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-40	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	I_D	-3.5 -2.8	A
Pulsed Drain Current		I_{DM}	-20	A
Continuous Source Current (Diode Conduction)		I_S	-1.2	A
Power Dissipation	$T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	P_D	1.20 0.81	W
Operation Junction Temperature		T_J	-55/150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	105	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

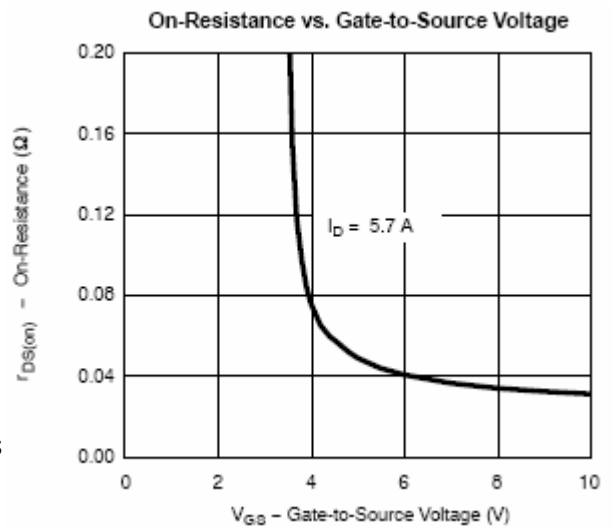
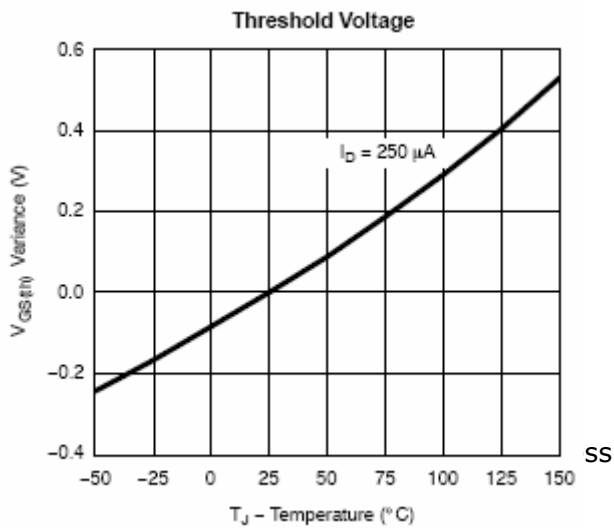
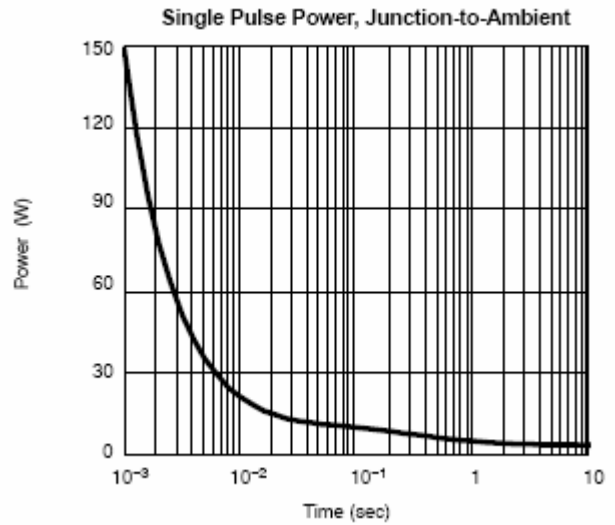
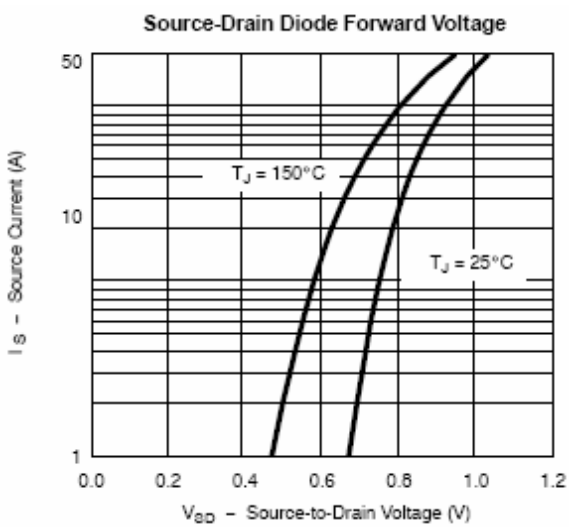
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-10\mu A$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.8		-2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-36V, V_{GS}=0V$			-1	uA
		$V_{DS}=-36V, V_{GS}=0V$ $T_J=85^\circ C$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -5V, V_{GS}=-4.5V$	-10			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3.0A$		0.075	0.081	Ω
		$V_{GS}=-4.5V, I_D=-2.8A$		0.105	0.112	
Forward Transconductance	g_{fs}	$V_{DS}=-15V, I_D=-3.0A$		13		S
Diode Forward Voltage	V_{SD}	$I_S=-1.3A, V_{GS}=0V$			-1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V$ $V_{GS}=-10V$ $I_D\equiv -3.0A$		9	12	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			2.0		
Input Capacitance	C_{iss}	$V_{DS}=-15V$ $V_{GS}=0V$ $F=1MHz$		500		pF
Output Capacitance	C_{oss}			95		
Reverse Transfer Capacitance	C_{rss}			50		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DD}=-15V$ $R_L=15\Omega$ $I_D=-1.0A$ $V_{GEN}=-10V$ $R_G=6\Omega$		8	20	nS
Turn-Off Time	$t_{d(off)}$ t_f			10	20	
				30	35	
				15	20	

TYPICAL CHARACTERISTICS (25°C Unless noted)



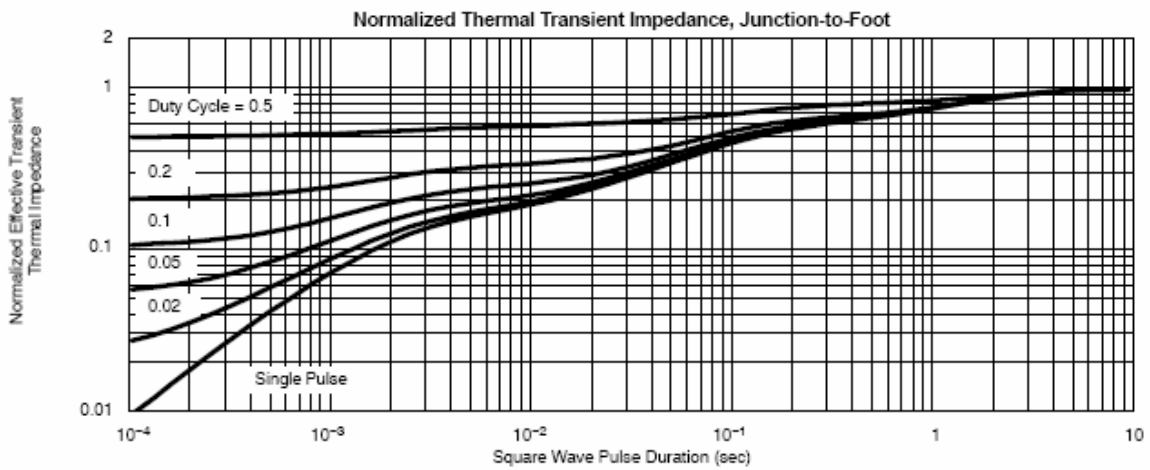
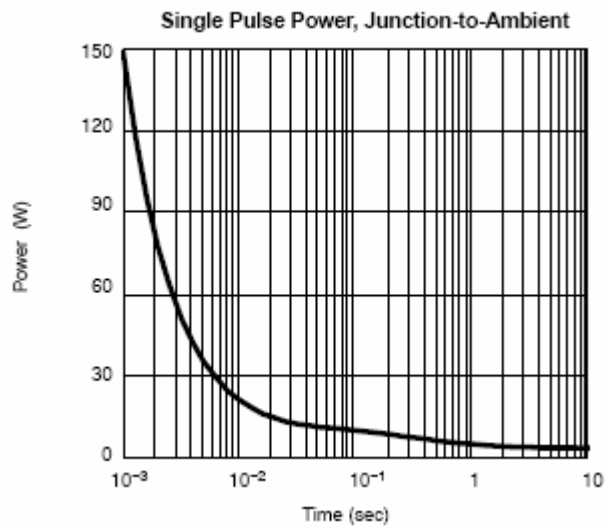
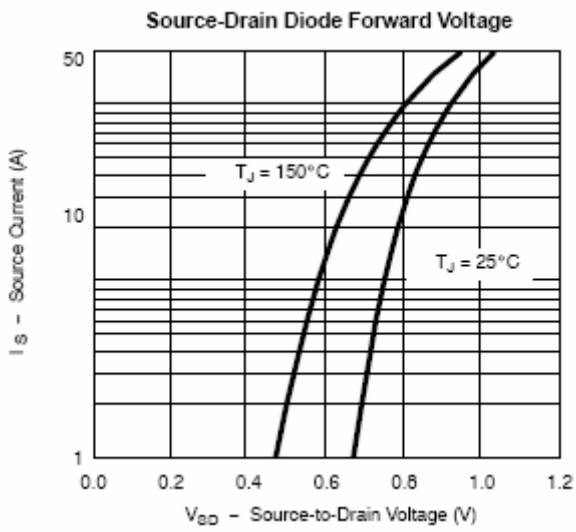
; nc

TYPICAL CHARACTERISTICS (25°C Unless noted)

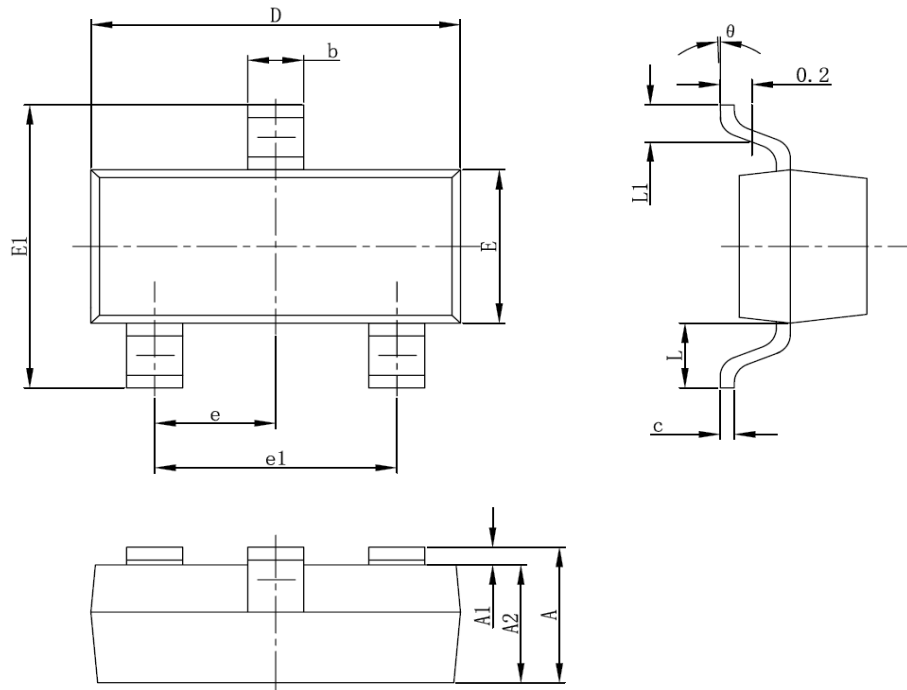


SS

TYPICAL CHARACTERISTICS (25°C Unless noted)



SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

